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TITLE: COIL FOR MAGNETIC INDUCTION ELEMENT

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ABSTRACT:

PURPOSE: To increase the current capacity of a coil for compact magnetic induction element such as transformer, inductor, etc., in combination with an integrated circuit device.

CONSTITUTION: This coil 30 is composed by a method wherein trench 31 deeply formed from the rear surface side of a semiconductor substrate 11 of a chip 10 on whose surface side another semiconductor device 20 such as integrated circuit device, etc., is formed is covered with an insulating film 32 so as to fill up the trench 31 with a high conductive metal such as

copper, etc., as a
coil conductor 33 by non-dielectrolytic plating step etc.
Furthermore, even if
the arrayal pitch of the coil conductor 33 is made minute
for miniaturization
of the magnetic induction element, the trench 31 can be
formed deeper if
necessary to increase the level of the coil conductor 22
while effectively
using the conventionally idling space on the rear surface
side of the substrate
11 thereby enabling the current capacity of the coil to be
increased.

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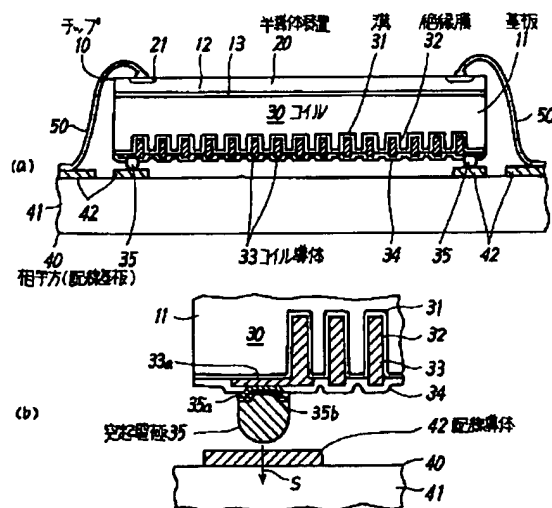
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(54)【発明の名称】 磁気誘導素子用コイル

(57) 【要約】

【目的】集積回路装置と組み合わせて用いる変圧器やインダクタ等の小形の磁気誘導素子のコイルの電流容量を向上させる。

【構成】集積回路装置等の半導体装置20が表面側に作り込まれるチップ10の半導体基板10の裏面側から溝31を深く掘り込んで溝面を絶縁膜32で覆い、コイル導体33として銅等の高導電性金属を無電解めっき法等によって溝31内に充填してコイル30を構成することにより、磁気誘導素子の小形化のためにコイル導体33の配列ピッチを微細化しても、基板11の裏側の従来に遊んでいたスペースを有効に利用しながら必要に応じて溝31を深く掘り込みコイル導体33の高さを増すことによりコイルの電流容量を向上できるようにする。



【特許請求の範囲】

【請求項1】半導体装置と組み合わせて用いられる磁気誘導素子のコイルであって、半導体装置用チップの基板の裏面側にコイルのパターンに掘り込まれた溝と、溝面を含むチップの裏面側に被着された絶縁膜と、絶縁膜で覆われた溝に充填された高導電性金属からなるコイル導体とを備え、コイル導体を突起電極を介して相手方の配線導体と接続して半導体装置とともに相手方に実装するようにしたことを特徴とする磁気誘導素子用コイル。

【請求項2】請求項1に記載のコイルにおいて、コイル導体が無電解めっきされた銅であることを特徴とする磁気誘導素子用コイル。

【請求項3】請求項1に記載のコイルにおいて、チップを実装する相手方の対向面側にコイルを設けるとともに実装面に磁性薄膜を配設し、チップ側および相手方側のコイルと磁性薄膜とにより磁気誘導素子を構成するようにしたことを特徴とする磁気誘導素子用コイル。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は安定化電源等に半導体装置と組み合わせて用いる小形のインダクタや変圧器である磁気誘導素子のコイルであって、集積回路装置等の半導体装置用のチップに作り込まれるものに関する。

【0002】

【従来の技術】安定化電源等の電子装置、例えばスイッチング電源やチョッパ制御装置では、従来はスイッチング用や整流用の個別半導体素子にインダクタ、変圧器等の磁気誘導素子やキャパシタ等の個別部品を組み合わせでプリント基板の上に実装する構造が主流であったが、用途拡大に伴い小形化の要求がとくに強いので最近ではこれに応じて半導体素子をチップのままセラミック配線基板に実装するいわゆるハイブリッド集積回路の構造が広く採用されるようになり、さらには大電力用の場合を除いてすべての個別半導体素子を制御回路とともに1個の集積回路装置のチップ内に集積化してしまうことも可能である。

【0003】このように半導体装置側の集積化が急速に進展しているのに対して個別部品、とくに磁気誘導素子の小形化は容易でなく、装置全体の体格を縮小して行く上で隘路になっている。従来、この磁気誘導素子の小形化は同じインダクタンスでも周波数に比例してリアクタンスが増加することを利用して、装置の動作周波数を高めることにより進めて来たが、1MHz以上ではインダクタンスの周波数特性が低下しやすいので、動作周波数をあまり高めても実効が上らず、むしろ高周波損失が増加して装置の全体効率の低下を招く結果になり兼ねない。

【0004】この難点を突破するため、磁気誘導素子を半導体プロセス技術を利用して微細パターン化した薄膜導体と磁性薄膜の積層構造にして思い切った小形化を図

り、同時に半導体チップ上に作り付けて集積回路装置と磁気誘導素子をワンチップ化する試みがなされておりその将来性が囁目されている。この薄膜積層構造の磁気誘導素子としては、渦巻き状やつづら折れ状コイルに形成した薄膜導体を1対の磁性薄膜で両側から挟み込む構造のものや、薄膜導体と磁性薄膜の条を織物状に入り組ませる構造が知られている。いずれの構造でも磁気誘導素子は外形寸法が10mm以下で厚みが数十 μ mの小形で偏平な形状なので、半導体装置のチップ上に半導体技術を利用して作り付けることができる。

【0005】

【発明が解決しようとする課題】上述の薄膜積層構造の磁気誘導素子は半導体技術を利用して薄膜導体のコイルパターンを微細化することにより著しい小形化を可能にし、同時にそのインダクタンスの周波数特性を向上して装置の動作周波数を1MHz以上に高め得る利点があるが、コイルを薄膜導体から形成するのでそのパターンの微細化を進めるほど導体幅が狭くなり、コイル導体に流し得る電流密度にはもちろん制約があるので磁気誘導素子の電流容量をあまり大きくできない問題がある。

【0006】この問題の解決には薄膜導体の厚みを増すしかないが、薄膜導体から相互間隔より高さが大なコイル導体をエッチングにより形成するのが容易でなく、大きな段差が付くのでその上に薄膜を積層するのが困難になり、かつコイルの放熱上も不利になって来る。本発明の目的は、かかる問題点を解決して半導体技術を利用しながら微細パターンに形成して容易に小形化でき、かつ電流容量を向上できる磁気誘導素子のコイルを得ることにある。

【0007】

【課題を解決するための手段】上記の目的は本発明によれば、半導体装置ないし集積回路装置が表面側に作り込まれるチップの半導体基板の裏面側に溝をコイル用パターンで深く掘り込み、この溝面を含む基板の裏面側に絶縁膜を被着し、絶縁膜で覆われた溝を充填するように高導電性金属からなるコイル導体を設け、コイル導体を突起電極を介して相手方の配線導体と接続して半導体装置とともにチップ実装するようにした磁気誘導素子のコイルにより達成される。

【0008】なお、上記の溝を良好な側面形状で深く掘り込むには、プラズマエッチング法ないしはリアクティブイオンエッチング法によるのが有利である。絶縁膜は酸化シリコン膜とするのが最も簡単かつ充分であり、これを基板のスチーム酸化等により付けることもできるが、チップの表面側に半導体装置がすでに作り込まれている場合は低温のCVD法により成膜するのがよい。溝内を充填するコイル導体用の高導電性金属には銅を用いるのがよく、その溝内への充填を良好にするにはこれが無電解めっきにより堆積するのが有利であり、さらにはこれを下地である溝面との密着性のよい低速無電解め

きと高速無電解めっきの2段階で堆積するのがとくに有利である。

【0009】上述のチップ実装に際してコイル導体を相手方の配線導体と接続する突起電極には、はんだのバンプ電極を用いるのが半導体装置を作り込んだチップの損傷を防止する上でとくに有利であり、突起電極はもちろんチップと相手方のいずれの側に設けてもよい。また、コイル導体の接続を確実にするためそれ用の高導電性金属からなる接続部をチップの基板の裏面上にコイル導体から延在させて設けておくのが有利である。

【0010】本発明の有利な実施ないしは適用上の態様では、チップを実装すべき相手方の対向面側にチップ側と同様な構造のコイルを設けるとともに、両者間の実装面に磁性薄膜を配設することによりチップ側および相手方側のコイルと磁性薄膜とによって磁気誘導素子が構成されるようにする。かかる態様では相手方の基板にはチップ側と同様に半導体を用いるのがよい。また、磁性薄膜はチップと相手方のいずれの側に設けてもよいが、相手方の表面を保護膜で覆い磁性薄膜をその上に担持させるのが有利である。

【0011】

【作用】前述の薄膜積層構造の磁気誘導素子はチップの半導体装置が作り込まれた方の表面側に積み重ね搭載されるが、本発明はチップの半導体基板の裏面側の遊んでいるスペースを有効に利用すればコイル導体の断面積を増加できる点に着目したもので、前項の構成にいう溝をこの基板の裏面側からコイル用の微細パターンで深く掘り込み、この溝面に絶縁膜を被着した上で溝を充填する高導電性金属からなるコイル導体を設けることにより、コイル導体の断面積を増加させてコイルの電流容量を向上し、同時にコイル導体の発熱を薄い絶縁膜を介して半導体基板に逃がすことによって放熱を良好にし、さらにコイル導体を突起電極を介して実装相手方の配線導体と接続することにより、コイル接続と同時に半導体装置を作り込んだチップの実装を果たせるようにしたものである。

【0012】

【実施例】以下、図を参照して本発明の実施例を説明する。図1は本発明の磁気誘導素子用コイルの一実施例を、図2はその異なる実施例をそれぞれチップおよび実装の相手方の断面図で示し、図3はチップ内に半導体装置とコイルを作り込む要領を主な工程ごとのチップの要部断面図で示すものである。なお、図1および図2の実施例では図の煩雑を避けるためコイルをインダクタ用とするが、変圧器用では例えば2個のコイルを入り組ませたパターンで作り込むことでよい。

【0013】図1(a)の上側に示されたチップ10はいわゆる基板接合形で、後に図3で説明するように半導体の1対の基板11と12が酸化膜13を介し相互に接合されている。上側の基板12は数十 μm の厚みに仕上げられ、例え

ば安定化電源のスイッチングトランジスタ、整流ダイオード等の回路素子と制御回路とを含む集積回路である半導体装置20がこれに作り込まれており、その外部との接続用に簡略に示された接続パッド21が周縁部に設けられる。本発明によるコイル30は下側の数百 μm の厚みの基板11の裏面側から作り込まれ、図1(b)に詳細を示すよう突起電極35を介して相手方40、図の例では配線基板のセラミック基板41上の配線導体42と接続される。本発明ではこの接続と同時にチップ10の相手方40への実装が果たされ、チップ10内の半導体装置20はその接続パッド21およびボンディング線50を介して相手方40の配線導体42と接続される。

【0014】本発明のコイル30は、チップ10の厚い方の基板11の裏面側から多数条の溝31を例えば30 μm 程度の細かな配列ピッチでそれぞれ深く掘り込み、その溝面を含む基板11の裏面側に例えば酸化シリコンの絶縁膜32を1 μm 程度の膜厚で被着し、かつ溝31内を充填する高導電性金属、例えば銅からなりかつ図示のようにかなり縦長な断面をもつコイル導体33を溝31に嵌め込むように設けてなる。溝31の幅は例えば20 μm とされ、その深さはコイル30に賦与すべき電流容量に応じて30 μm 程度以上とされる。この図1の実施例ではコイル30のパターンは図の左右方向に並ぶその導体33が図の前後で交互に折り返すつづら折れ状とされ、図示のようにその左右の端部で相手方40と接続される。

【0015】図1(b)はこの接続部を拡大断面で示す。突起電極35はコイル30と相手方40のいずれの側に設けてもよいが、この実施例では前者側に設けかつはんだのバンプ電極とする。図のように基板11の裏面をコイル導体33上を含め窒化シリコン等の保護膜34で覆い、それに開口した窓の中でコイル30に接続するよう突起電極35を設ける。コイル導体33の幅が狭いのでそれ用の銅を側方に延出して接続部33aとする。通例のようにこの接続部33aと保護膜34の窓内で接触する薄いチタン等の下地膜35aと銅等の下地膜35bを付け、その上側にはんだを電解めっき法で成長させ、かつ先端に丸みがつくようリフローさせて突起電極35用のバンプとする。かかるはんだバンプの突起電極35は相手方40の配線導体42に対し図では矢印Sで示す300°C以下の低温のはんだ付けにより容易に接続できる。

【0016】図2の実施例のチップ10は図1と同様な構造であるがその裏面側のコイル30が渦巻き状パターンとされる。この実施例の相手方60は図1と異なりその基板61を半導体基板とし、その上面のチップ10の実装部分にそれと同じ構造のコイル30を設けてチップ10側のコイル30と直列接続する。そのため、この相手方60のコイル導体33の上を層間絶縁膜62で覆い、その上側にアルミ等の配線導体63を配設し、さらにその上を覆う保護膜64の窓内で配線導体63と接続するように突起電極65を突設し、かつ窓内に露出させた配線導体63を接続パッド66とす

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る。図示の例では相手方60のコイル30の中央の端部は配線導体63と突起電極65を介してチップ10のコイル30の中央端部と接続され、相手方60のコイル30の左側の端部はその接続部33aを介して接続パッド66と接続されている。

【0017】さらにこの図2の実施例ではチップ10と相手方60の相互間に磁性薄膜70を配設して両者のコイル30とともにいわゆる内鉄形の磁気誘導素子、この例ではインダクタを構成する。この磁性薄膜70は軟磁性をもつ強磁性体金属をスパッタ法等により10〜数十 μm の膜厚に成膜してフォトリソエッチングによって所望のパターンに形成することでよく、チップ10と相手方60のいずれの側に設けてもよいが、図の例ではチップ10側にはコイル導体33が露出しているの、相手方60の方に設けてその表面を覆う保護膜64上に担持させる。図2に示されたその他の部分は図1と同じなので説明を省略する。

【0018】以上説明した図1と図2のいずれの実施例においても、コイル30のパターンを微細化しても基板11に数百 μm の厚みがあるので、必要に応じて溝31を深く掘り込んでコイル導体33の高さを増すことにより、コイル30の電流容量を従来の数倍以上に向上できる。また、チップ10の表面側の半導体装置20がコイル導体33から図のようになんまり離れているので、薄膜積層構造に比べてコイル30の電流により発生する磁場の悪影響を受けるおそれを減少させることができる。

【0019】次に、図3を参照してチップ10内に半導体装置20とコイル30を作り込む要領を説明する。図3(a)〜(d)は基板12を半導体装置20の回路素子や回路部分を作り込むべき半導体領域に分離する工程を示し、図3(e)〜(h)は基板11の裏面からコイル30を作り込む工程を示す。これら工程はすべてウエハの状態で行われるので符号10は今までのチップのかわりにウエハを示すものとし、このウエハ10はいわゆる誘電体分離ウエハであるものとする。また、図3(e)以降では基板11がその裏面を上側に向けた姿勢で示されている。

【0020】図3(a)は基板接合工程であって、1対の基板11と12のいずれか一方の表面に酸化膜13を付けて鏡面に仕上げた後、両基板11と12を重ね合わせた状態で不活性雰囲気内の高温加熱により両者を接合してウエハ10とし、かつ基板12に研磨を施して半導体装置20を作り込むに適した数十 μm の厚みに仕上げる。それ以降はこの基板12の誘電体分離工程であり、まずその最初の図3(b)の工程では溝14をプラズマエッチング法により基板12の表面から酸化膜13に達するまで掘り込んで基板12を複数の半導体領域15に分離し、かつ溝面を含む全面をスチーム酸化法による1 μm 程度の膜厚の酸化膜である誘電体膜16で被覆する。

【0021】図3(c)は多結晶シリコンによる溝の充填工程であり、シラン等を原料ガスとする熱CVD法により多結晶シリコン17をウエハ10の全面上に堆積させて溝

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14を充填する。この際、半導体領域15の上側にも多結晶シリコン17が堆積するので、次の図3(d)の工程ではウエハ10の表面上の多結晶シリコン17を酸化することにより酸化膜18に変え、かつ必要に応じてそれを所定の厚みにまでエッチングして図示の状態とする。以上によって例えばn形の基板12が誘電体膜16により相互に絶縁された複数の半導体領域15に誘電体分離されるので、以降は前述の半導体装置20である集積回路を構成する回路素子や回路部分がこれらの半導体領域15に振り分けて作り込まれる。

【0022】コイル30を作り込むための最初の工程である図3(e)では、ウエハ10の裏側の基板11の表面から溝31をエッチングにより図のように深く掘り込む。この溝31はもちろんコイル用の微細パターンに形成されたフォトリソレジスト膜をマスクとして掘り込まれるが、その際のエッチングは SF_6 と酸素を含むガス中のプラズマエッチング法、とくにリアクティブイオンエッチング法によるのがよく、これにより例えば20 μm 幅と狭くかつ30 μm 以上の深い溝31を基板11の表面に対して垂直でかつ良好な側面形状で掘り込むことができる。

【0023】次の図3(f)の工程では溝31の溝面を含む基板11の全面を1 μm 程度の膜厚の絶縁膜32で覆う。この絶縁膜32は基板12側に半導体装置20が作り込まれる以前の場合は1100 $^{\circ}\text{C}$ の高温下のスチーム酸化法で付けるのがよいが、半導体装置20が作り込まれた以後の場合はシランと酸素を反応ガスとする200 $^{\circ}\text{C}$ 程度の低温下のプラズマCVD法によって成膜するのがよい。

【0024】図3(g)の工程では溝31内にコイル導体33用の高導電性金属を充填する。この金属には銅を用い2段階の無電解めっき法で成長させるのがよい。最初は下地と密着性のよい低速の無電解めっきとし、硫酸銅、ロッシェル塩、フォルムアルデヒド、苛性ソーダ、シアン化ナトリウム等を含むめっき液により20 $^{\circ}\text{C}$ の温度下で薄く銅を成長させ、次に硫酸銅、EDTA 2Na、フォルムアルデヒド、苛性ソーダ、シアン化ナトリウムを含むめっき液を用いるめっき速度が約1桁高い高速無電解めっきにより、70 $^{\circ}\text{C}$ 程度の温度下で銅を溝31内に充填しかつ図のように基板11の全面を覆うように成長させる。

【0025】最後の図3(h)の工程ではコイル導体33用の金属をエッチングしてコイル30を完成する。この工程ではフォトリソレジスト膜をマスクMとし例えば塩酸液を用いる化学エッチングにより銅をコイル30用の所定のパターンに形成し、かつ図示の例では基板11の表面上に銅の一部を残してコイル30の端部用の接続部33aとする。これ以降は図1のようにコイル30側に突起電極35を設ける場合はコイル導体33を保護膜34で被覆するのがよいが、図2のようにコイル導体33を露出させたままでも差し支えない。

【0026】以上説明した実施例に限らず、本発明は種々の態様で実施することができる。例えば、実施例では

チップ内の半導体装置が作り込まれる基板部分を誘電体分離構造としたが、接合分離構造としてもよい。溝のコイル導体用金属による充填も実施例の無電解めっきに限らず蒸着、電解めっき等ないしそれらの組み合わせによっても可能である。磁性薄膜とコイルとの配置構造にも自由度があって、磁気誘導素子がインダクタか変圧器かによっても種々な選択が可能であり、あるいは磁性薄膜をチップ内部に組み入れることも可能である。

【0027】

【発明の効果】以上のとおり本発明の磁気誘導素子用コイルでは、半導体装置ないし集積回路装置が表面側に作り込まれるチップの半導体基板の裏面側に溝を深く掘り込み、この溝面を含む基板の裏面側に絶縁膜を被着し、絶縁膜で覆われた溝を充填するように高導電性金属からなるコイル導体を設け、コイル導体を突起電極を介して相手方の配線導体と接続して半導体装置とともにチップ実装することによって、次の効果を上げることができる。

【0028】(a) チップの半導体基板の裏面側のスペースを有効利用してコイルを作り込むので、小形化のためコイルパターンを微細化しても数百 μm の厚みの基板に溝を深く掘り込んでコイル導体の高さを増すことにより、コイルの電流容量を従来の数倍以上に向上することができる。

(b) コイル導体を櫛歯状に切った溝に嵌め込む構造なのでその発熱をごく薄い絶縁膜を介して半導体基板に逃がすことができ、従来の薄膜導体と磁性薄膜とを絶縁膜を介して積み上げる薄膜積層構造に比べて放熱効果を良好にし、コイルの電流容量を一層向上させることができる。

【0029】(c) コイル導体を突起電極を介して実装相手方の配線導体と接続すると同時に半導体装置を作り込んだチップの実装を果たすことができるので、安定化電源等の組み立てに要する手間を大幅に省くことができる。

(d) チップ表面側の半導体装置がコイル導体からかなり離れているので、薄膜積層構造に比べて半導体装置がコイル電流により発生する磁場の悪影響を受けるおそれを

減少させることができる。

【0030】なお、本発明のコイルは半導体装置とともに相手方に対しチップ実装する方式なので安定化電源等を完全にはワンチップ化できないが、実装相手方をチップと大差がない程度に小形化することができる。

【図面の簡単な説明】

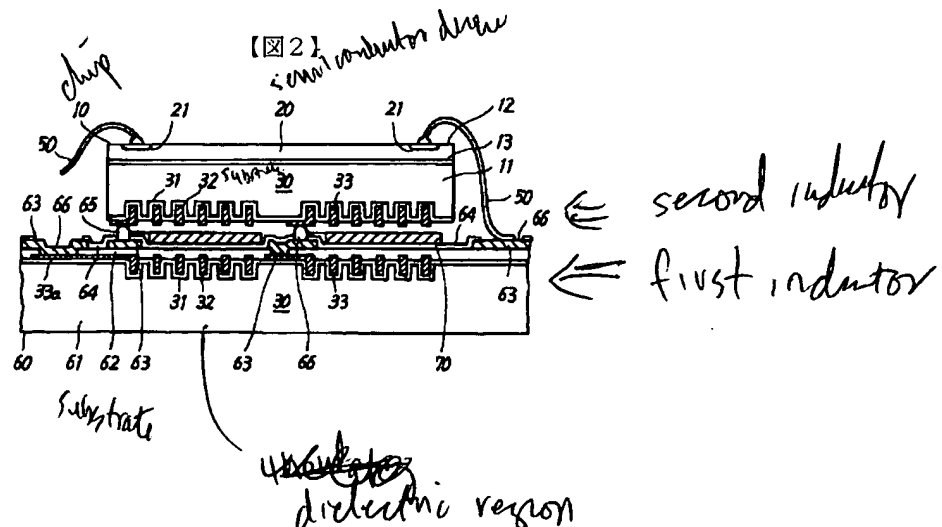
【図1】本発明の磁気誘導素子用コイルの実施例を示し、同図(a)はチップとその実装相手方の断面図、同図(b)はその要部拡大断面図である。

【図2】本発明の磁気誘導素子用コイルの異なる実施例を示すチップとその実装相手方の断面図である。

【図3】チップ内に半導体装置とコイルを作り込む要領を主な工程ごとの状態で示し、同図(a)は基板接合工程、同図(b)は誘電体分離溝の掘り込みと誘電体膜の被着工程、同図(c)は多結晶シリコンの成長工程、同図(d)は半導体領域への誘電体分離の完成工程、同図(e)はコイル用の溝の掘り込み工程、同図(f)は絶縁膜の被着工程、同図(g)はコイル導体用金属による溝充填工程、同図(h)はコイルの完成工程のそれぞれ状態を示すチップ用ウエハの要部断面図である。

【符号の説明】

- | | |
|--------|------------------|
| 10 | チップないしはそれ用のウエハ |
| 11 | 半導体基板 |
| 20 | 半導体装置ないしは集積回路装置 |
| 21 | 半導体装置の接続パッド |
| 30 | 磁気誘導素子用コイル |
| 31 | 溝 |
| 32 | 絶縁膜 |
| 33 | コイル導体 |
| 30 33a | コイルの接続部 |
| 35 | 突起電極ないしはバンプ電極 |
| 40 | チップが実装される相手方 |
| 42 | 配線導体 |
| 50 | 半導体装置の接続用ボンディング線 |
| 60 | チップが実装される相手方 |
| 62 | 配線導体 |
| 65 | 突起電極ないしはバンプ電極 |
| 70 | 磁気誘導素子用磁性薄膜 |



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NOTICES *

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1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. **** shows the word which can not be translated.

3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The slot which is the coil of a magnetic-induction component used combining a semiconductor device, and was dug deep by the pattern of a coil at the rear-face side of the substrate of the chip for semiconductor devices, It has a conductor. the coil which consists of a high conductivity metal with which the insulator layer put on the rear-face side of the chip containing a groove surface and the slot covered by the insulator layer were filled up -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the other party -- the coil for magnetic-induction components characterized by connecting with a conductor and mounting in the other party with a semiconductor device.

[Claim 2] a coil according to claim 1 -- setting -- a coil -- the coil for magnetic-induction components characterized by a conductor being copper by which nonelectrolytic plating was carried out.

[Claim 3] The coil for magnetic-induction components characterized by arranging a magnetic thin film in a component side while preparing a coil in the opposed face side of the other party who mounts a chip in a coil according to claim 1, and constituting a magnetic-induction component with the coil and magnetic thin film by the side of the tip side and the other party.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention is the coil of the magnetic-induction component which is the small inductor and transformer which are used for a regulated power supply etc. combining a semiconductor device, and relates to what is made by the chip for semiconductor devices, such as an integrated circuit device.

[0002]

[Description of the Prior Art] Electronic instruments, such as a regulated power supply, with switching power supply or chopper control equipment, it is an inductor to the individual semiconductor device the object for switching, and for rectification conventionally, Although the structure mounted on a printed circuit board combining discrete part, such as magnetic-induction components, such as a transformer, and a capacitor, was in use The structure of the so-called hybrid integrated circuit of mounting a semiconductor device in a ceramic wiring board according to this with application expansion with a chip recently since especially the demand of a miniaturization is strong comes to be adopted widely. It is also possible to integrate all individual semiconductor devices in one chip of an integrated circuit device with a control circuit except for the case further for large power.

[0003] Thus, to progressing quickly, especially the miniaturization of a magnetic-induction component is not easy, and integration by the side of a semiconductor device is ****, when reducing the physique of the whole equipment and going, discrete part and. A result which efficiency does not go up even if it raises

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clock frequency not much, since the frequency characteristics of an inductance tend to fall above 1MHz, although advanced by raising the clock frequency of equipment using a reactance increasing in proportion to a frequency also at the inductance with the same miniaturization of this former and magnetic-induction component, but RF loss increases rather, and causes the decline in the whole equipment effectiveness may be brought.

[0004] In order to break through this difficulty, it is made the laminated structure of the thin film conductor which carried out the detailed patternizing of the magnetic-induction component using the semi-conductor process technique, and a magnetic thin film, and the attempt which attains a radical miniaturization, fixes on a semiconductor chip at coincidence, and one-chip-izes an integrated circuit device and a magnetic-induction component is made, and it is ** carried out of those possibilities. The structure of making the thing of structure and ** of a thin film conductor and a magnetic thin film which put the thin film conductor formed in the letter coil of a curled form fellow face crease from both sides with one pair of magnetic thin films as a magnetic-induction component of this thin film laminated structure becoming intricate in the shape of textiles is known. With any structure, since it is the small and flat configuration which is dozens of micrometers thin at 10mm or less, a dimension can fix a magnetic-induction component on the chip of a semiconductor device using semiconductor technology.

[0005]

[Problem(s) to be solved by the Invention] Although the magnetic-induction component of an above-mentioned thin film laminated structure has the advantage which enables a remarkable miniaturization, improves the frequency characteristics of the inductance to coincidence, and can raise the clock frequency of equipment to 1MHz or more by making the coil pattern of a thin film conductor detailed using semiconductor technology since a coil is formed from a thin film conductor, so that detailed-ization of the pattern is advanced -- a conductor width -- narrow -- becoming -- a coil -- natural to the current density which can be passed to a conductor -- since there is constraint, there is a problem which can seldom enlarge current capacity of a magnetic-induction component.

[0006] although the thickness of a thin film conductor must be increased for solution of this problem -- a size [spacing / a thin film conductor to / mutual] height coil -- since a level difference that it is not easy to form a conductor by etching and big is attached, it becomes difficult to carry out the laminating of the thin film on it, and the heat dissipation top of a coil also becomes disadvantageous. The purpose of this invention is to obtain the coil of the magnetic-induction component which can form in a detailed pattern, and can be miniaturized easily, solving this trouble and using semiconductor technology, and can improve current capacity.

[0007]

[Means for Solving the Problem] According to this invention, the above-mentioned purpose digs a slot deep deeply by the pattern for coils to the rear-face side of the semi-conductor substrate of the chip with which a semiconductor device thru/or an integrated circuit device are made at a front-face side. A conductor is prepared. the coil which consists of a high conductivity metal so that it may be filled up with the slot which put the insulator layer on the rear-face side of the substrate containing this groove surface, and was covered by the insulator layer -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the other party -- it is attained by the coil of the magnetic-induction component which connects with a conductor and was made to carry out chip mounting with a semiconductor device.

[0008] In addition, in order to dig the above-mentioned slot deep deeply in a good side-face configuration, it is advantageous to be based on the plasma-etching method or the reactive-ion-etching method. As for an insulator layer, considering as the silicon oxide film is easy and most enough, and although this can also be attached by steam oxidization of a substrate etc., when a semiconductor device is already made at the front-face side of a chip, it is good to form membranes with a low-temperature CVD method. the coil filled up with Mizouchi -- it is good to use copper for the high conductivity metal for conductors, and it is advantageous to deposit this on making restoration to the Mizouchi good with nonelectrolytic plating, and it is advantageous especially to deposit this further in two steps, the good low-speed nonelectrolytic plating of adhesion with the groove surface which is a substrate, and high-speed nonelectrolytic plating.

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[0009] above-mentioned chip mounting -- facing -- a coil -- a conductor -- wiring of the other party -- especially when using the bump electrode of solder prevents damage on the chip which made the semiconductor device, it is advantageous to the projection electrode linked to a conductor, and a projection electrode is natural -- you may prepare in which [of a chip and the other party] side. moreover, a coil -- the connection which consists of a high conductivity metal for them in order to ensure connection of a conductor -- the rear-face top of the substrate of a chip -- a coil -- it is advantageous to make it extend from a conductor and to prepare.

[0010] while preparing the coil of the same structure as the tip side in the opposed face side of the other party who should mount a chip, a magnetic-induction component is constituted from the mode on advantageous operation of this invention, or application by arranging a magnetic thin film in the component side between both by the coil and magnetic thin film by the side of the tip side and the other party. In this mode, it is good for the other party's substrate to use a semi-conductor like the tip side. Moreover, although a magnetic thin film may be prepared in which [of a chip and the other party] side, it is advantageous to cover the other party's front face by the protective coat, and to make a magnetic thin film support on it.

[0011]

[Function] Although the magnetic-induction component of the above-mentioned thin film laminated structure is accumulated and carried in the front-face side of the direction where the semiconductor device of a chip was made It is what noted the point which can increase the cross section of a conductor. if this invention uses effectively the tooth space where the rear-face side of the semi-conductor substrate of a chip is lying idle -- a coil -- the coil which consists of a high conductivity metal filled up with a slot after digging deep deeply the slot said to the configuration of the preceding clause by the detailed pattern for coils from the rear-face side of this substrate and putting an insulator layer on this groove surface -- by preparing a conductor Heat dissipation is made good by missing generation of heat of a conductor to a semi-conductor substrate through a thin insulator layer. a coil -- the cross section of a conductor is increased -- making -- the current capacity of a coil -- improving -- coincidence -- a coil -- further -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the mounting other party -- it enables it to achieve mounting of the chip which made coil connection, simultaneously a semiconductor device by connecting with a conductor

[0012]

[Example] Hereafter, the example of this invention is explained with reference to drawing. In drawing 1 , drawing 2 shows the different example for one example of the coil for magnetic-induction components of this invention with the sectional view of the other party of a chip and mounting, respectively, and drawing 3 shows the point which makes a semiconductor device and a coil in a chip with the important section sectional view of the chip for every main processes. in addition -- although a coil is made into inductors in the example of drawing 1 and drawing 2 in order to avoid **** of drawing -- the object for transformers -- if -- for example, it is good by making from the pattern which made two coils become intricate.

[0013] Drawing 1 (a) The chip 10 shown in the bottom is the so-called substrate junction type, and one pair of substrates 11 and 12 of a semi-conductor are mutually joined through the oxide film 13 so that drawing 3 may explain later. The connection pad 21 with which the semiconductor device 20 which is the integrated circuit which the thickness of dozens of micrometers is made to the upper substrate 12, for example, includes a circuit element and control circuits, such as a switching transistor of a regulated power supply and rectifier diode, was made by this, and was shown simple in connection with the exterior is formed in the periphery section. the coil 30 by this invention is made from the rear-face side of the lower substrate 11 with a thickness of hundreds of micrometers -- having -- drawing 1 (b) a detail is shown -- as -- the projection electrode 35 -- minding -- the example of the other party 40 and drawing -- wiring on the ceramic substrate 41 of a wiring substrate -- it connects with a conductor 42. in this invention, mounting to the other party 40 of this connection, simultaneously a chip 10 achieves -- having -- the semiconductor device 20 in a chip 10 -- that connection pad 21 and the bonding line 50 -- minding -- wiring of the other party 40 -- it connects with a conductor 42.

[0014] The slot 31 of several articles is deeply dug deep by the about 30-micrometer fine array pitch, respectively. the coil 30 of this invention -- from the rear-face

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side of the substrate 11 of the thicker one of a chip 10 -- many -- the coil which has a quite longwise cross section like [it consists of a high conductivity metal which puts the insulator layer 32 of silicon oxide on the rear-face side of the substrate 11 containing the groove surface by about 1-micrometer thickness, and is filled up with the inside of a slot 31, for example, copper, and] illustration -- it prepares and becomes so that a conductor 33 may be inserted in a slot 31. width of face of a slot 31 is set to 20 micrometers, and the depth is set to about 30 micrometers or more according to the current capacity which should be endowed with a coil 30. In the example of this drawing 1, the pattern of a coil 30 is made into the letter of a ** face crease which that conductor 33 on a par with the longitudinal direction of drawing turns up by turns before and behind drawing, and is connected with the other party 40 at the edge of those right and left like illustration.

[0015] Drawing 1 (b) An enlarged section shows this connection. Although the projection electrode 35 may be formed in which [of a coil 30 and the other party 40] side, in this example, it is prepared in a former side and let it be the bump electrode of solder. drawing -- like -- the rear face of a substrate 11 -- a coil -- it covers by the protective coats 34, such as silicon nitride, including a conductor 33 top, and the projection electrode 35 is formed so that it may connect with a coil 30 in the aperture which carried out opening to it. a coil -- since the width of face of a conductor 33 is narrow, it extends to the side and the copper for them is set to connection 33a. A reflow is carried out and it considers as the bump for projection electrode 35 so that substrate film 35a, such as thin titanium, and substrate film 35b, such as copper, which contact this connection 33a within the aperture of a protective coat 34 like usually may be attached, and solder may be grown up into that bottom by the electrolysis galvanizing method and a radius of circle may stick at a tip. this solder bump's projection electrode 35 -- wiring of the other party 40 -- an arrow head S shows to a conductor 42 by a diagram It is easily connectable with soldering of low temperature 300 degrees C or less.

[0016] Although the chip 10 of the example of drawing 2 is the same structure as drawing 1, let the coil 30 by the side of the rear face be a curled form pattern. Unlike drawing 1, the other party 60 of this example uses that substrate 61 as a semi-conductor substrate, forms the coil 30 of the structure same into the mounting part of the chip 10 of that top face as it, and does series connection to the coil 30 by the side of a chip 10. therefore, this other party's 60 coil -- a conductor 33 top -- an interlayer insulation film 62 -- covering -- that top -- wiring of aluminum etc. -- a conductor 63 -- arranging -- further -- a it top -- the inside of the aperture of the wrap protective coat 64 -- wiring -- wiring to which it protruded on and the projection electrode 65 was exposed in the aperture so that it might connect with a conductor 63 -- let a conductor 63 be the connection pad 66. the example of illustration -- the edge of the center the other party's 60 coil 30 -- wiring -- it connects with the central edge of the coil 30 of a chip 10 through a conductor 63 and the projection electrode 65, and the edge on the left-hand side of the other party's 60 coil 30 is connected with the connection pad 66 through the connection 33a.

[0017] Furthermore in the example of this drawing 2, a magnetic thin film 70 is arranged between a chip 10 and the other party 60, and it is the so-called magnetic-induction component of core type in both coil 30, An inductor consists of this example. the ferromagnetic metal in which this magnetic thin film 70 has soft magnetism -- a spatter etc. -- 10- although it is possible to form membranes to dozens of micrometers thickness, and to form in a desired pattern by photo etching and you may prepare in which [of a chip 10 and the other party 60] side -- the example of drawing -- a chip 10 side -- a coil -- since the conductor 33 is exposed, it prepares in the other party's 60 direction, and that front face is made to support on the wrap protective coat 64 Since the other parts shown in drawing 2 are the same as drawing 1, explanation is omitted.

[0018] since the thickness of hundreds of micrometers is in a substrate 11 also in which example of drawing 1 explained above and drawing 2 even if it makes the pattern of a coil 30 detailed -- the need -- responding -- a slot 31 -- deep -- digging deep -- a coil -- the current capacity of a coil 30 can be improved several or more times over the past by increasing the height of a conductor 33. moreover, the semiconductor device 20 by the side of the front face of a chip 10 -- a coil -- since it is considerably separated from the conductor 33 as shown in drawing, a

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possibility of receiving the bad influence of the magnetic field generated according to the current of a coil 30 compared with a thin film laminated structure can be decreased.

[0019] Next, the point which makes a semiconductor device 20 and a coil 30 in a chip 10 with reference to drawing 3 is explained. Drawing 3 (a) - (d) The process which divides a substrate 12 into the semiconductor region which should make the circuit element and circuit part of a semiconductor device 20 is shown, and it is drawing 3 (e). - (h) The process which makes a coil 30 from the rear face of a substrate 11 is shown. Since all of these processes are advanced in the state of a wafer, a sign 10 shall show a wafer instead of an old chip, and this wafer 10 shall be the so-called dielectric separation wafer. Moreover, drawing 3 (e) The substrate 11 is shown by henceforth by the posture which turned the rear face to the bottom.

[0020] Drawing 3 (a) It is a substrate junction process, after attaching the oxide film 13 to one front face of one pair of substrates 11 and 12 and making a mirror plane, where both the substrates 11 and 12 are piled up, both are joined by the heating at high temperature in inactive ambients, and it considers as a wafer 10, and the thickness of dozens of micrometers suitable for grinding to a substrate 12 and making a semiconductor device 20 is made. It is the dielectric separation process of this substrate 12 after it, and it is that first drawing 3 (b) first. The dielectric film 16 which is an oxide film of the about 1-micrometer thickness by the steam oxidation style covers at a process the whole surface which digs a slot 14 deep until it reaches an oxide film 13 from the front face of a substrate 12 by the plasma-etching method, divides a substrate 12 into two or more semiconductor regions 15, and contains a groove surface.

[0021] Drawing 3 (c) It is the packer of the slot by polycrystalline silicon, and polycrystalline silicon 17 is made to deposit on the whole surface of a wafer 10 with the heat CVD method which makes a silane etc. material gas, and it is filled up with a slot 14. Under the present circumstances, since polycrystalline silicon 17 accumulates also on the semiconductor region 15 bottom, it is following drawing 3 (d). At a process, by oxidizing the polycrystalline silicon 17 on the front face of a wafer 10, it changes into an oxide film 18, and it is etched even into predetermined thickness if needed, and it considers as the condition of illustration. Since dielectric separation of the substrate 12 of n form is carried out by the above in two or more semiconductor regions 15 mutually insulated with the dielectric film 16, the circuit element and circuit part which constitute the integrated circuit which is the above-mentioned semiconductor device 20 distribute to these semiconductor regions 15, and are made henceforth.

[0022] drawing 3 (e) which is the process of the beginning for making a coil 30 **** -- from the front face of the substrate 11 on the background of a wafer 10, by etching, a slot 31 is deeply dug deep, as shown in drawing. For this slot 31, although the photoresist film formed in the natural detailed pattern for coils is dug deep as a mask, etching in that case is SF6. The plasma-etching method in the gas containing oxygen and being based especially on the reactive-ion-etching method can dig the trench 31 30 micrometers or more deep in a perpendicular and good side-face configuration to the front face of a substrate 11 as narrowly [it is good and /, for example] by this as 20-micrometer width of face.

[0023] Following drawing 3 (f) At a process, the whole surface of the substrate 11 containing the groove surface of a slot 31 is covered by the insulator layer 32 of about 1-micrometer thickness. This insulator layer 32 makes a silane and oxygen reactant gas, when it is, after making a semiconductor device 20 for ** with sufficient attaching with the steam oxidation style under a 1100-degree C elevated temperature when it is, before making a semiconductor device 20 at a substrate 12 side. It is good to form membranes by the plasma-CVD method under about 200-degree C low temperature.

[0024] drawing 3 (g) a process -- the inside of a slot 31 -- a coil -- it is filled up with the high conductivity metal for conductors 33. It is good for this metal to make it grow up by two steps of nonelectrolytic plating methods using copper. Consider as the nonelectrolytic plating of the good low speed of a substrate and adhesion at first, and copper is thinly grown up under the temperature of 20 degrees C with the plating liquid containing a copper sulfate, a Rochell salt, formaldehyde, caustic alkali of sodium, a sodium cyanide, etc. Next, the inside of a slot 31 is filled up with the bottom of the temperature of about 70 degrees C for copper, and it is made to grow up with high-speed nonelectrolytic plating with the plating rate

Untitled

high a figure single [about] using the plating liquid containing a copper sulfate, EDTA 2Na, formaldehyde, caustic alkali of sodium, and a sodium cyanide, so that the whole surface of a substrate 11 may be covered, as shown in drawing.

[0025] the last drawing 3 (h) a process -- a coil -- the metal for conductors 33 is etched and a coil 30 is completed. At this process, the photoresist film is used as Mask M, copper is formed in the predetermined pattern for coils 30 by the chemical etching using hydrochloric-acid liquid, and it leaves copper [some] on the front face of a substrate 11 in the example of illustration, and is referred to as connection 33a for the edges of a coil 30. the case where the projection electrode 35 is formed in a coil 30 side like drawing 1 after this -- a coil -- although it is good to cover a conductor 33 with a protective coat 34 -- drawing 2 -- like -- a coil -- even if it uses it, with the conductor 33 exposed, it does not interfere.

[0026] Not only an example but this invention explained above can be carried out in various modes. For example, although the substrate part by which the semiconductor device in a chip is made from an example was made into dielectric isolation construction, it is good also as junction isolation structure. the coil of a slot -- a conductor -- public funds -- restoration by the group is also possible not only by the nonelectrolytic plating of an example but those combination, such as vacuum evaporation and electrolysis plating. It is able for there to be a degree of freedom also in the arrangement structure of a magnetic thin film and a coil, and for a magnetic-induction component to be possible for various selections, or to include a magnetic thin film in the interior of a chip with an inductor or a transformer.

[0027]

[Effect of the Invention] As above, with the coil for magnetic-induction components of this invention A slot is deeply dug deep to the rear-face side of the semi-conductor substrate of the chip with which a semiconductor device thru/or an integrated circuit device are made at a front-face side. A conductor is prepared. the coil which consists of a high conductivity metal so that it may be filled up with the slot which put the insulator layer on the rear-face side of the substrate containing this groove surface, and was covered by the insulator layer -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the other party -- the following effectiveness can be raised by connecting with a conductor and carrying out chip mounting with a semiconductor device.

[0028] (a) since the tooth space by the side of the rear face of the semi-conductor substrate of a chip is used effectively and a coil is made, even if it makes a coil pattern detailed for a miniaturization -- a substrate with a thickness of hundreds of micrometers -- a slot -- deep -- digging deep -- a coil -- the current capacity of a coil can be improved several or more times over the past by increasing the height of a conductor.

(b) a coil -- since it is the structure of inserting a conductor in the slot cut in the shape of a ctenidium, the generation of heat can be missed to a semi-conductor substrate through a very thin insulator layer, compared with the thin film laminated structure which accumulates a conventional thin film conductor and a conventional magnetic thin film through an insulator layer, the heat dissipation effectiveness can be made good, and the current capacity of a coil can be raised further.

[0029] (c) a coil -- a conductor -- a projection electrode -- minding -- wiring of the mounting other party -- since mounting of the chip which made the semiconductor device can be achieved while connecting with a conductor, the time and effort which assemblies, such as a regulated power supply, take can be saved sharply.

(d) the semiconductor device by the side of a chip front face -- a coil -- since it is considerably separated from the conductor, a possibility of receiving the bad influence of the magnetic field which a semiconductor device generates according to a coil current compared with a thin film laminated structure can be decreased.

[0030] In addition, although-izing of the regulated power supply etc. cannot be completely carried out [one chip] since the coil of this invention is the method which carries out chip mounting to the other party with a semiconductor device, the mounting other party can be miniaturized in extent without a chip and great difference.

[Translation done.]

Untitled

TECHNICAL FIELD

[Industrial Application] This invention is the coil of the magnetic-induction component which is the small inductor and transformer which are used for a regulated power supply etc. combining a semiconductor device, and relates to what is made by the chip for semiconductor devices, such as an integrated circuit device.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Electronic instruments, such as a regulated power supply, with switching power supply or chopper control equipment It is an inductor to the individual semiconductor device the object for switching, and for rectification conventionally, Although the structure mounted on a printed circuit board combining discrete part, such as magnetic-induction components, such as a transformer, and a capacitor, was in use The structure of the so-called hybrid integrated circuit of mounting a semiconductor device in a ceramic wiring board according to this with application expansion with a chip recently since especially the demand of a miniaturization is strong comes to be adopted widely. It is also possible to integrate all individual semiconductor devices in one chip of an integrated circuit device with a control circuit except for the case further for large power.

[0003] Thus, to progressing quickly, especially the miniaturization of a magnetic-induction component is not easy, and integration by the side of a semiconductor device is ****, when reducing the physique of the whole equipment and going, discrete part and. A result which efficiency does not go up even if it raises clock frequency not much, since the frequency characteristics of an inductance tend to fall above 1MHz, although advanced by raising the clock frequency of equipment using a reactance increasing in proportion to a frequency also at the inductance with the same miniaturization of this former and magnetic-induction component, but RF loss increases rather, and causes the decline in the whole equipment effectiveness may be brought.

[0004] In order to break through this difficulty, it is made the laminated structure of the thin film conductor which carried out the detailed patternizing of the magnetic-induction component using the semi-conductor process technique, and a magnetic thin film, and the attempt which attains a radical miniaturization, fixes on a semiconductor chip at coincidence, and one-chip-izes an integrated circuit device and a magnetic-induction component is made, and it is ** carried out of those possibilities. The structure of making the thing of structure and ** of a thin film conductor and a magnetic thin film which put the thin film conductor formed in the letter coil of a curled form fellow face crease from both sides with one pair of magnetic thin films as a magnetic-induction component of this thin film laminated structure becoming intricate in the shape of textiles is known. With any structure, since it is the small and flat configuration which is dozens of micrometers thin at 10mm or less, a dimension can fix a magnetic-induction component on the chip of a semiconductor device using semiconductor technology.

[Translation done.]

EFFECT OF THE INVENTION

Untitled

[Effect of the Invention] with the coil for magnetic-induction components of this invention, it is as above, the coil which consists of a high conductivity metal so that it may be filled up with the slot where the semiconductor device thru/or the integrated circuit device dug the slot deep deeply to the rear-face side of the semi-conductor substrate of the chip made at a front-face side, put the insulator layer on the rear-face side of the substrate containing this groove surface, and was covered by the insulator layer -- a conductor -- preparing -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the other party -- the following effectiveness can raise by connecting with a conductor and carrying out chip mounting with a semiconductor device.

[0028] (a) since the tooth space by the side of the rear face of the semi-conductor substrate of a chip is used effectively and a coil is made, even if it makes a coil pattern detailed for a miniaturization -- a substrate with a thickness of hundreds of micrometers -- a slot -- deep -- digging deep -- a coil -- the current capacity of a coil can be improved several or more times over the past by increasing the height of a conductor.

(b) a coil -- since it is the structure of inserting a conductor in the slot cut in the shape of a ctenidium, the generation of heat can be missed to a semi-conductor substrate through a very thin insulator layer, compared with the thin film laminated structure which accumulates a conventional thin film conductor and a conventional magnetic thin film through an insulator layer, the heat dissipation effectiveness can be made good, and the current capacity of a coil can be raised further.

[0029] (c) a coil -- a conductor -- a projection electrode -- minding -- wiring of the mounting other party -- since mounting of the chip which made the semiconductor device can be achieved while connecting with a conductor, the time and effort which assemblies, such as a regulated power supply, take can be saved sharply.

(d) the semiconductor device by the side of a chip front face -- a coil -- since it is considerably separated from the conductor, a possibility of receiving the bad influence of the magnetic field which a semiconductor device generates according to a coil current compared with a thin film laminated structure can be decreased.

[0030] In addition, although-izing of the regulated power supply etc. cannot be completely carried out [one chip] since the coil of this invention is the method which carries out chip mounting to the other party with a semiconductor device, the mounting other party can be miniaturized in extent without a chip and great difference.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be solved by the Invention] Although the magnetic-induction component of an above-mentioned thin film laminated structure has the advantage which enables a remarkable miniaturization, improves the frequency characteristics of the inductance to coincidence, and can raise the clock frequency of equipment to 1MHz or more by making the coil pattern of a thin film conductor detailed using semiconductor technology since a coil is formed from a thin film conductor, so that detailed-ization of the pattern is advanced -- a conductor width -- narrow -- becoming -- a coil -- natural to the current density which can be passed to a conductor -- since there is constraint, there is a problem which can seldom enlarge current capacity of a magnetic-induction component.

[0006] although the thickness of a thin film conductor must be increased for solution of this problem -- a size [spacing / a thin film conductor to / mutual] height coil -- since a level difference that it is not easy to form a conductor by etching and big is attached, it becomes difficult to carry out the laminating of the thin film on it, and the heat dissipation top of a coil also becomes disadvantageous. The purpose of this invention is to obtain the coil of the magnetic-induction component which can form in a detailed pattern, and can be miniaturized easily, solving this trouble and using semiconductor technology, and

can improve current capacity.

[Translation done.]

MEANS

[Means for Solving the Problem] According to this invention, the above-mentioned purpose digs a slot deep deeply by the pattern for coils to the rear-face side of the semi-conductor substrate of the chip with which a semiconductor device thru/or an integrated circuit device are made at a front-face side. A conductor is prepared. the coil which consists of a high conductivity metal so that it may be filled up with the slot which put the insulator layer on the rear-face side of the substrate containing this groove surface, and was covered by the insulator layer -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the other party -- it is attained by the coil of the magnetic-induction component which connects with a conductor and was made to carry out chip mounting with a semiconductor device.

[0008] In addition, in order to dig the above-mentioned slot deep deeply in a good side-face configuration, it is advantageous to be based on the plasma-etching method or the reactive-ion-etching method. As for an insulator layer, considering as the silicon oxide film is easy and most enough, and although this can also be attached by steam oxidization of a substrate etc., when a semiconductor device is already made at the front-face side of a chip, it is good to form membranes with a low-temperature CVD method. the coil filled up with Mizouchi -- it is good to use copper for the high conductivity metal for conductors, and it is advantageous to deposit this on making restoration to the Mizouchi good with nonelectrolytic plating, and it is advantageous especially to deposit this further in two steps, the good low-speed nonelectrolytic plating of adhesion with the groove surface which is a substrate, and high-speed nonelectrolytic plating.

[0009] above-mentioned chip mounting -- facing -- a coil -- a conductor -- wiring of the other party -- especially when using the bump electrode of solder prevents damage on the chip which made the semiconductor device, it is advantageous to the projection electrode linked to a conductor, and a projection electrode is natural -- you may prepare in which [of a chip and the other party] side. moreover, a coil -- the connection which consists of a high conductivity metal for them in order to ensure connection of a conductor -- the rear-face top of the substrate of a chip -- a coil -- it is advantageous to make it extend from a conductor and to prepare.

[0010] while preparing the coil of the same structure as the tip side in the opposed face side of the other party who should mount a chip, a magnetic-induction component is constituted from the mode on advantageous operation of this invention, or application by arranging a magnetic thin film in the component side between both by the coil and magnetic thin film by the side of the tip side and the other party. In this mode, it is good for the other party's substrate to use a semi-conductor like the tip side. Moreover, although a magnetic thin film may be prepared in which [of a chip and the other party] side, it is advantageous to cover the other party's front face by the protective coat, and to make a magnetic thin film support on it.

[Translation done.]

OPERATION

[Function] Although the magnetic-induction component of the above-mentioned thin film laminated structure is accumulated and carried in the front-face side of the direction where the semiconductor device of a chip was made It is what noted the

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point which can increase the cross section of a conductor. if the tooth space where the rear-face side of the semi-conductor substrate of a chip is lying idle is effectively used in this invention -- a coil -- the coil which consists of a high conductivity metal filled up with a slot after digging deep deeply the slot said to the configuration of the preceding clause by the detailed pattern for coils from the rear-face side of this substrate and putting an insulator layer on this groove surface -- a conductor is prepared. therefore, a coil -- the cross section of a conductor is increased -- making -- the current capacity of a coil -- improving -- coincidence -- a coil -- missing generation of heat of a conductor to a semi-conductor substrate through a thin insulator layer -- heat dissipation -- good -- carrying out -- further -- a coil -- a conductor -- a projection electrode -- minding -- wiring of the mounting other party -- it enables it to achieve mounting of the chip which made coil connection, simultaneously a semiconductor device by connecting with a conductor

[Translation done.]

EXAMPLE

[Example] Hereafter, the example of this invention is explained with reference to drawing. In drawing 1, drawing 2 shows the different example for one example of the coil for magnetic-induction components of this invention with the sectional view of the other party of a chip and mounting, respectively, and drawing 3 shows the point which makes a semiconductor device and a coil in a chip with the important section sectional view of the chip for every main processes. in addition -- although a coil is made into inductors in the example of drawing 1 and drawing 2 in order to avoid **** of drawing -- the object for transformers -- if -- for example, it is good by making from the pattern which made two coils become intricate.

[0013] Drawing 1 (a) The chip 10 shown in the bottom is the so-called substrate junction type, and one pair of substrates 11 and 12 of a semi-conductor are mutually joined through the oxide film 13 so that drawing 3 may explain later. The connection pad 21 with which the semiconductor device 20 which is the integrated circuit which the thickness of dozens of micrometers is made to the upper substrate 12, for example, includes a circuit element and control circuits, such as a switching transistor of a regulated power supply and rectifier diode, was made by this, and was shown simple in connection with the exterior is formed in the periphery section. the coil 30 by this invention is made from the rear-face side of the lower substrate 11 with a thickness of hundreds of micrometers -- having -- drawing 1 (b) a detail is shown -- as -- the projection electrode 35 -- minding -- the example of the other party 40 and drawing -- wiring on the ceramic substrate 41 of a wiring substrate -- it connects with a conductor 42. in this invention, mounting to the other party 40 of this connection, simultaneously a chip 10 achieves -- having -- the semiconductor device 20 in a chip 10 -- that connection pad 21 and the bonding line 50 -- minding -- wiring of the other party 40 -- it connects with a conductor 42.

[0014] The slot 31 of several articles is deeply dug deep by the about 30-micrometer fine array pitch, respectively. the coil 30 of this invention -- from the rear-face side of the substrate 11 of the thicker one of a chip 10 -- many -- the coil which has a quite longwise cross section like [it consists of a high conductivity metal which puts the insulator layer 32 of silicon oxide on the rear-face side of the substrate 11 containing the groove surface by about 1-micrometer thickness, and is filled up with the inside of a slot 31, for example, copper, and] illustration -- it prepares and becomes so that a conductor 33 may be inserted in a slot 31. width of face of a slot 31 is set to 20 micrometers, and the depth is set to about 30 micrometers or more according to the current capacity which should be endowed with a coil 30. In the example of this drawing 1, the pattern of a coil 30 is made into the letter of a ** face crease which that conductor 33 on a par with the longitudinal direction of drawing turns up by turns before and behind drawing, and is connected with the other party 40 at the edge of those right and left like

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illustration.

[0015] Drawing 1 (b) An enlarged section shows this connection. Although the projection electrode 35 may be formed in which [of a coil 30 and the other party 40] side, in this example, it is prepared in a former side and let it be the bump electrode of solder. drawing -- like -- the rear face of a substrate 11 -- a coil -- it covers by the protective coats 34, such as silicon nitride, including a conductor 33 top, and the projection electrode 35 is formed so that it may connect with a coil 30 in the aperture which carried out opening to it. a coil -- since the width of face of a conductor 33 is narrow, it extends to the side and the copper for them is set to connection 33a. A reflow is carried out and it considers as the bump for projection electrode 35 so that substrate film 35a, such as thin titanium, and substrate film 35b, such as copper, which contact this connection 33a within the aperture of a protective coat 34 like usually may be attached, and solder may be grown up into that bottom by the electrolysis galvanizing method and a radius of circle may stick at a tip. this solder bump's projection electrode 35 -- wiring of the other party 40 -- an arrow head S shows to a conductor 42 by a diagram It is easily connectable with soldering of low temperature 300 degrees C or less.

[0016] Although the chip 10 of the example of drawing 2 is the same structure as drawing 1, let the coil 30 by the side of the rear face be a curled form pattern. Unlike drawing 1, the other party 60 of this example uses that substrate 61 as a semi-conductor substrate, forms the coil 30 of the structure same into the mounting part of the chip 10 of that top face as it, and does series connection to the coil 30 by the side of a chip 10. therefore, this other party's 60 coil -- a conductor 33 top -- an interlayer insulation film 62 -- covering -- that top -- wiring of aluminum etc. -- a conductor 63 -- arranging -- further -- a it top -- the inside of the aperture of the wrap protective coat 64 -- wiring -- wiring to which it protruded on and the projection electrode 65 was exposed in the aperture so that it might connect with a conductor 63 -- let a conductor 63 be the connection pad 66. the example of illustration -- the edge of the center the other party's 60 coil 30 -- wiring -- it connects with the central edge of the coil 30 of a chip 10 through a conductor 63 and the projection electrode 65, and the edge on the left-hand side of the other party's 60 coil 30 is connected with the connection pad 66 through the connection 33a.

[0017] Furthermore in the example of this drawing 2, a magnetic thin film 70 is arranged between a chip 10 and the other party 60, and it is the so-called magnetic-induction component of core type in both coil 30, An inductor consists of this example. the ferromagnetic metal in which this magnetic thin film 70 has soft magnetism -- a spatter etc. -- 10- although it is possible to form membranes to dozens of micrometers thickness, and to form in a desired pattern by photo etching and you may prepare in which [of a chip 10 and the other party 60] side -- the example of drawing -- a chip 10 side -- a coil -- since the conductor 33 is exposed, it prepares in the other party's 60 direction, and that front face is made to support on the wrap protective coat 64 Since the other parts shown in drawing 2 are the same as drawing 1, explanation is omitted.

[0018] since the thickness of hundreds of micrometers is in a substrate 11 also in which example of drawing 1 explained above and drawing 2 even if it makes the pattern of a coil 30 detailed -- the need -- responding -- a slot 31 -- deep -- digging deep -- a coil -- the current capacity of a coil 30 can be improved several or more times over the past by increasing the height of a conductor 33. moreover, the semiconductor device 20 by the side of the front face of a chip 10 -- a coil -- since it is considerably separated from the conductor 33 as shown in drawing, a possibility of receiving the bad influence of the magnetic field generated according to the current of a coil 30 compared with a thin film laminated structure can be decreased.

[0019] Next, the point which makes a semiconductor device 20 and a coil 30 in a chip 10 with reference to drawing 3 is explained. Drawing 3 (a) - (d) The process which divides a substrate 12 into the semiconductor region which should make the circuit element and circuit part of a semiconductor device 20 is shown, and it is drawing 3 (e). - (h) The process which makes a coil 30 from the rear face of a substrate 11 is shown. Since all of these processes are advanced in the state of a wafer, a sign 10 shall show a wafer instead of an old chip, and this wafer 10 shall be the so-called dielectric separation wafer. Moreover, drawing 3 (e) The substrate 11 is shown by henceforth by the posture which turned the rear face to the bottom.

Untitled .

[0020] Drawing 3 (a) It is a substrate junction process, after attaching the oxide film 13 to one front face of one pair of substrates 11 and 12 and making a mirror plane, where both the substrates 11 and 12 are piled up, both are joined by the heating at high temperature in inactive ambients, and it considers as a wafer 10, and the thickness of dozens of micrometers suitable for grinding to a substrate 12 and making a semiconductor device 20 is made. It is the dielectric separation process of this substrate 12 after it, and it is that first drawing 3 (b) first. The dielectric film 16 which is an oxide film of the about 1-micrometer thickness by the steam oxidation style covers at a process the whole surface which digs a slot 14 deep until it reaches an oxide film 13 from the front face of a substrate 12 by the plasma-etching method, divides a substrate 12 into two or more semiconductor regions 15, and contains a groove surface.

[0021] Drawing 3 (c) It is the packer of the slot by polycrystalline silicon, and polycrystalline silicon 17 is made to deposit on the whole surface of a wafer 10 with the heat CVD method which makes a silane etc. material gas, and it is filled up with a slot 14. Under the present circumstances, since polycrystalline silicon 17 accumulates also on the semiconductor region 15 bottom, it is following drawing 3 (d). At a process, by oxidizing the polycrystalline silicon 17 on the front face of a wafer 10, it changes into an oxide film 18, and it is etched even into predetermined thickness if needed, and it considers as the condition of illustration. Since dielectric separation of the substrate 12 of n form is carried out by the above in two or more semiconductor regions 15 mutually insulated with the dielectric film 16, the circuit element and circuit part which constitute the integrated circuit which is the above-mentioned semiconductor device 20 distribute to these semiconductor regions 15, and are made henceforth.

[0022] drawing 3 (e) which is the process of the beginning for making a coil 30 **** -- from the front face of the substrate 11 on the background of a wafer 10, by etching, a slot 31 is deeply dug deep, as shown in drawing. For this slot 31, although the photoresist film formed in the natural detailed pattern for coils is dug deep as a mask, etching in that case is SF6. The plasma-etching method in the gas containing oxygen and being based especially on the reactive-ion-etching method can dig the trench 31 30 micrometers or more deep in a perpendicular and good side-face configuration to the front face of a substrate 11 as narrowly [it is good and /, for example] by this as 20-micrometer width of face.

[0023] Following drawing 3 (f) At a process, the whole surface of the substrate 11 containing the groove surface of a slot 31 is covered by the insulator layer 32 of about 1-micrometer thickness. This insulator layer 32 makes a silane and oxygen reactant gas, when it is, after making a semiconductor device 20 for ** with sufficient attaching with the steam oxidation style under a 1100-degree C elevated temperature when it is, before making a semiconductor device 20 at a substrate 12 side. It is good to form membranes by the plasma-CVD method under about 200-degree C low temperature.

[0024] drawing 3 (g) a process -- the inside of a slot 31 -- a coil -- it is filled up with the high conductivity metal for conductors 33. It is good for this metal to make it grow up by two steps of nonelectrolytic plating methods using copper. Consider as the nonelectrolytic plating of the good low speed of a substrate and adhesion at first, and copper is thinly grown up under the temperature of 20 degrees C with the plating liquid containing a copper sulfate, a Rochell salt, formaldehyde, caustic alkali of sodium, a sodium cyanide, etc. Next, the inside of a slot 31 is filled up with the bottom of the temperature of about 70 degrees C for copper, and it is made to grow up with high-speed nonelectrolytic plating with the plating rate high a figure single [about] using the plating liquid containing a copper sulfate, EDTA 2Na, formaldehyde, caustic alkali of sodium, and a sodium cyanide, so that the whole surface of a substrate 11 may be covered, as shown in drawing.

[0025] the last drawing 3 (h) a process -- a coil -- the metal for conductors 33 is etched and a coil 30 is completed. At this process, the photoresist film is used as Mask M, copper is formed in the predetermined pattern for coils 30 by the chemical etching using hydrochloric-acid liquid, and it leaves copper [some] on the front face of a substrate 11 in the example of illustration, and is referred to as connection 33a for the edges of a coil 30. the case where the projection electrode 35 is formed in a coil 30 side like drawing 1 after this -- a coil -- although it is good to cover a conductor 33 with a protective coat 34 -- drawing 2 -- like -- a coil -- even if it uses it, with the conductor 33 exposed, it does not interfere.

Untitled

[0026] Not only an example but this invention explained above can be carried out in various modes. For example, although the substrate part by which the semiconductor device in a chip is made from an example was made into dielectric isolation construction, it is good also as junction isolation structure. the coil of a slot -- a conductor -- public funds -- restoration by the group is also possible not only by the nonelectrolytic plating of an example but those combination, such as vacuum evaporation and electrolysis plating. It is able for there to be a degree of freedom also in the arrangement structure of a magnetic thin film and a coil, and for a magnetic-induction component to be possible for various selections, or to include a magnetic thin film in the interior of a chip with an inductor or a transformer.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The example of the coil for magnetic-induction components of this invention is shown, and it is this drawing (a). A chip, the mounting other party's sectional view, and this drawing (b) It is the important section expanded sectional view.

[Drawing 2] They are the chip in which the example from which the coil for magnetic-induction components of this invention differs is shown, and the mounting other party's sectional view.

[Drawing 3] The point which makes a semiconductor device and a coil in a chip is shown in the condition for every main processes. This drawing (a) A substrate junction process and this drawing (b) A dig lump of a dielectric separation slot and the covering process of a dielectric film, This drawing (c) The growth process of polycrystalline silicon, and this drawing (d) The completion process of the dielectric separation to a semiconductor region, this drawing (e) the slot for coils -- digging deep -- a process and this drawing (f) The covering process of an insulator layer, and this drawing (g) a coil -- a conductor -- public funds -- like the slot packer by the group -- this drawing (h) each of the completion process of a coil -- it is the important section sectional view of the wafer for a chip in which a condition is shown.

[Description of Notations]

- 10 Chip or Wafer for Them
- 11 Semi-conductor Substrate
- 20 Semiconductor Device or Integrated Circuit Device
- 21 Connection Pad of Semiconductor Device
- 30 Coil for Magnetic-Induction Components
- 31 Slot
- 32 Insulator Layer
- 33 Coil -- Conductor
- 33a The connection of a coil
- 35 Projection Electrode or Bump Electrode
- 40 Other Party by Whom Chip is Mounted
- 42 Wiring -- Conductor
- 50 Bonding Line for Connection of Semiconductor Device
- 60 Other Party by Whom Chip is Mounted
- 62 Wiring -- Conductor
- 65 Projection Electrode or Bump Electrode
- 70 Magnetic Thin Film for Magnetic-Induction Components

[Translation done.]